Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A semiconductor package, comprising:

a lead frame having a first side and a second side, and formed with a die pad and a plurality of leads surrounding the die pad, wherein the leads are each defined into an inner lead, an outer lead and a middle portion positioned between the inner lead and the outer lead, and each of the middle portions extends outwardly at sides thereof to form protrusions for reducing spacing between the adjacent middle portions of the leads;

an encapsulant for encapsulating the middle portions of the leads and the second side of the lead frame with the outer leads being exposed, wherein a cavity is formed in the encapsulant for exposing the die pad and the inner leads on the first side of the lead frame, allowing a semiconductor chip and bonding wires to be received in the cavity, and preventing flash of a resin compound that forms the encapsulant on the exposed die pad and the inner leads due to the reduced spacing between the adjacent middle portions of the leads;

the semiconductor chip mounted in the cavity on the die pad of the first side of the lead frame;

the plurality of bonding wires formed in the cavity for electrically connecting the semiconductor chip to the inner leads of the lead frame; and

a lid adhered onto the encapsulant for covering an opening of the cavity.

Claim 2 (original): The semiconductor package of claim 1, wherein the middle portions of the leads are arranged in a manner that spacing between the adjacent middle portions is 0.10 mm, or equal to or smaller than 0.15mm.

Claim 3 (original): The semiconductor package of claim 1, further comprising a first tape adhered to the second side of the lead frame.

Claim 4 (original): The semiconductor package of claim 3, further comprising a second tape adhered to the first side of the lead frame in a manner free of interference with arrangement of the bonding wires.

Claim 5 (withdrawn): A method for fabricating a semiconductor package, comprising the steps of:

providing a lead frame having a first side and a second side, wherein the lead frame is formed with a die pad and a plurality of leads surrounding the die pad, and the leads are each defined into an inner lead, an outer lead and a middle portion positioned between the inner lead and the outer lead, with each of the middle portions extending outwardly at sides thereof to form protrusions;

forming an encapsulant to encapsulate the lead frame with the outer leads being exposed, wherein a cavity is formed in the encapsulant for exposing the die pad and the inner leads on the first side of the lead frame, allowing a semiconductor chip and bonding wires to be received in the cavity;

mounting a semiconductor chip in the cavity on the die pad of the first side of the lead frame;

forming a plurality of bonding wires in the cavity to electrically connect the semiconductor chip to the inner leads of the lead frame; and

adhering a lid onto the encapsulant to cover an opening of the cavity.

Claim 6 (withdrawn): The method of claim 5, wherein the middle portions of the leads are arranged in a manner that spacing between the adjacent middle portions is 0.10 mm, or equal to or smaller than 0.15mm.

Claim 7 (withdrawn): The method of claim 5, further comprising a step of adhering a first tape to the second side of the lead frame prior to the step of forming the encapsulant.

Claim 8 (withdrawn): The method of claim 7, further comprising a step of adhering a second tape to the first side of the lead frame in a manner free of interference with arrangement of the bonding wires prior to the step of forming the encapsulant.